What is claimed is:

1. A data processing device comprising:

a cache memory;

a cache control part for controlling the cache memory; and

a memory control part accessible to a memory in response to a cache mishit of the cache memory,

wherein in having access to a memory burstable in response to a cache mishit, the memory control part forms first information for indicating a burst length of the memory and it can control a single or plurality of burst operations necessary to obtain a data length meeting a cache line length according to the first information, and

the cache control part can control a cache fill operation of filling data acquired in the single or plurality of burst operations in the cache memory so as to locate the data in order of addresses according to the first information.

2. The data processing device according to claim 1, wherein in the cache fill operation, the cache control part receives inputs of address information in a cache mishit, the first information, and a synchronization signal synchronous with a delimiter of data acquired in burst operations by the memory control part, and the cache control part generates a cache fill

address for determining a data order of cache fill in synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meant by the first information.

3. The data processing device according to claim 1, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the memory control part controls a burst operation starting from a top of a boundary of a data block defined by the burst length in subsequent burst operations.

4. A data processing system comprising:

a data processing device having a CPU and a cache memory; and

a memory connected to the data processing device, the memory being burstable and configuring a main memory for the cache memory,

wherein the cache memory has a cache line length of L bytes,

the memory is burstable in a range of a burst length in bytes, where L times one over two to the n-th power (n is a

natural number), and

the data processing device forms first information for indicating a burst length of the memory to a cache line length of the cache memory in response to a cache mishit of the cache memory, the data processing device allows the memory into burst operations for a single or plurality of times necessary to obtain a data length meeting the cache line length according to the first information, and the data processing device performs control of returning data of L bytes thereby obtained to the cache memory so as to arrange the data in order of addresses according to the first information.

5. A data processing system comprising:

a data processing device having a CPU and a cache memory; and

a plurality of memories connected to the data processing device, the plurality of memories being burstable and configuring a main memory for the cache memory,

wherein the cache memory has a cache line length of L bytes,

the plurality of memories is burstable in a range of a burst length in bytes, where L times one over two to the n-th power (n is a natural number), and the burst length is allowed to be set in each of the plurality of memories by the data processing device, and

the data processing device establishes a memory with data in a cache mishit as an object to be accessed in response to a cache mishit of the cache memory, and the data processing device performs control in which the data processing device forms first information for indicating a burst length of the memory to be accessed to a cache line length of the cache memory, the data processing device allows the memory into burst operations for a single or plurality of times necessary to obtain a data length meeting the cache line length according to the first information, and the data processing device returns data of L bytes thereby obtained so as to locate the data in order of addresses according to the first information.

6. The data processing system according to claim 4 or 5, wherein the data processing device performs control in which data acquired in the burst operations for the single or plurality of times is filled in the cache memory according to the first information.

7. The data processing system according to claim 4 or 5, wherein in cache fill operation, the data processing device generates a synchronization signal synchronous with a delimiter of data acquired from the memory in the burst operations, and the data processing device generates a cache fill address for determining a data order of cache fill in

synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meant by the first information.

8. The data processing system according to claim 4 or 5, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent bust operations.

9. A data processing system comprising:

a CPU;

a cache memory accessible by the CPU;

a cache control part for controlling the cache memory;

a memory control part accessible to a memory in response to a cache mishit of the cache memory; and

a memory connected to the memory control part, the memory being burstable,

wherein in having access to the memory in response to a cache mishit, the memory control part generates first information for indicating a burst length of the memory to a

cache line length of the cache memory, and the memory control part can control a single or plurality of burst operations necessary to obtain a data length meeting the cache line length according to the first information, and

the cache control part can control a cache fill operation of filling data acquired in the single or plurality of burst operations in the cache memory so as to locate the data in order of addresses by wraparound according to the first information.

10. The data processing system according to claim 9, wherein in the cache fill operation the cache control part receives inputs of address information in a cache mishit, the first information, and a synchronization signal synchronous with a delimiter of data acquired in the burst operation by the memory control part, the cache control part controls wraparound starting from the address information in a range of a burst length meant by the first information, and the cache control part generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal.

11. The data processing system according to claim 10, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the memory control part controls a burst operation by wraparound starting from a data location at an address in the cache mishit in a first burst operation,

and the memory control part controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.

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